REMARKS

Claims 9 and 37 have been amended. No claims have been added or cancelled. Therefore, claims 1-41 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

Section 112, First Paragraph, Rejection:

The Examiner rejected claim 10 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Specifically, the Examiner asserts that the claim states that a dispatch unit stores a microcode trace to a read only memory and that it is unclear how this is possible since a read only memory by definition can only be read from and not stored to. The Examiner further asserts that since the specification does not disclose how the dispatch unit can store to a read only memory, claim 10 is not enabled and the phrase "read only memory" was interpreted as "memory" for the remainder of his examination. Applicants respectfully traverse this rejection. Claim 10 did not recite storing one or more microcode traces to a ROM, as in a write operation, but instead recited that the dispatch unit stores (i.e., contains) the microcode subroutine in one or more microcode traces in a ROM. This claim and the original claim 9 are clearly supported in the specification in paragraphs [0010] and [0048], among others. However, in order to expedite prosecution, claim 9 has been amended to recite, "The microprocessor of claim 1, wherein the microcode subroutine is stored as one or more microcode traces." Therefore, claim 10, as it depends from claim 9, now recites that the microcode subroutine is stored as one or more microcode traces within a read only memory. Thus, it would be clear to one skilled in the art that claim 10 does not recite writing to a read only memory.

For at least the reasons above, Applicants assert that the subject matter of claim 10 is supported in the specification in such a way as to enable one skilled in the art to which it pertains to make and/or use the invention. Therefore, Applicants respectfully request the removal of the rejection of claim 10 under 35 U.S.C. § 112, first paragraph.

Section 102(b) Rejections:

The Examiner rejected claims 1, 15-17, 27-29, 39 and 41 under 35 U.S.C. § 102(b) as being anticipated by Tran (U.S. Patent 5,864,689), and claim 40 as being anticipated by Carbine et al. (U.S. Patent 5,630,083) (hereinafter "Carbine"). Applicants respectfully traverse these rejections for at least the following reasons.

Regarding claim 1, contrary to the Examiner's assertion, Tran fails to teach or suggest *a scheduler coupled to the dispatch unit and configured to schedule dispatched operations for execution, wherein in response to receiving a microcoded instruction, the dispatch unit is configured to dispatch to the scheduler a microcode subroutine call operation that includes a tag identifying a microcode subroutine associated with the microcoded instruction.* The Examiner cites column 8, line 55 – column 9, line 4, and Tran's target address therein, as teaching *wherein in response to receiving a microcoded instruction, the dispatch unit is configured to dispatch to the scheduler a microcode subroutine call operation that includes a tag identifying a microcode subroutine associated with the microcoded instruction.* However, this citation does not describe Tran's microcode unit 45 and instruction decode unit 36 (which the Examiner equates with Applicants' dispatch unit) dispatching to a reservation station (which the Examiner equates with Applicants' scheduler) a microcode subroutine call, including the limitations recited in claim 1. Instead, this citation describes, "when instruction decode unit 36 detects an instruction corresponding to a routine within microcode unit 45, an indication of the instruction is transferred upon instruction indication bus 62 to microcode unit 45" and also "the indication may comprise the target address of a subroutine call instruction." An indication of an instruction, even one that includes a target address of a subroutine call instruction, is not itself a microcode subroutine call, as recited in claim 1.

Furthermore, this citation describes that when instruction decode unit 36 detects a microcoded instruction, it sends an indication of the instruction to microcode unit 45. It does not describe dispatching a microcode subroutine call operation *to a scheduler*, as

recited in claim 1. Note that according to Tran, the indication of the instruction is sent to microcode unit 45, not to Tran's reservation station (which the Examiner equates to the scheduler of claim 1). Tran's microcode unit 45 is not a scheduler. In fact, column 8, lines 61-64 goes on to describe that if instruction decode unit 36 detects an instruction to be performed by microcode unit 45, it stalls (i.e., stops dispatching instructions) until microcode unit 45 completes the corresponding routine.

Applicants remind the Examiner that anticipation requires the presence in a single prior art reference disclosure of each and every limitation of the claimed invention, arranged as in the claim. M.P.E.P 2131; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). As discussed above, Tran fails to disclose *in response to receiving a microcoded instruction, the dispatch unit is configured to dispatch to the scheduler a microcode subroutine call operation that includes a tag identifying a microcode subroutine associated with the microcoded instruction.* Therefore, Tran cannot be said to anticipate claim 1.

For at least the reasons above, the rejection of claim 1 is not supported by the cited art and removal thereof is respectfully requested.

Claim 17 includes limitations similar to claim 1, and so the arguments presented above apply with equal force to this claim, as well.

Regarding claim 29, contrary to the Examiner's assertion, Tran fails to teach or suggest *detecting a microcoded instruction within the stream of instructions, wherein the microcoded instruction immediately precedes an other instruction in program order, in response to said detecting, dispatching a microcode subroutine call operation that identifies a microcode subroutine associated with the microcoded instruction.* The Examiner cites column 4, lines 36-41, as teaching detecting a microcoded instruction that immediately precedes another instruction in program order. However, this citation

describes that if instruction decode unit 36 detects an instruction to be performed by microcode unit 45, it stalls (i.e., stops dispatching instructions) until microcode unit 45 indicates that the routine corresponding to that instruction has completed dispatch. This citation says nothing about the microcoded instruction immediately preceding another instruction in program order, as recited in Applicants' claim 29.

Further regarding claim 29, the Examiner cites column 8, line 55 – column 9, line 4, as teaching dispatching a microcode subroutine call operation in response to detecting the microcoded instruction. However, this citation does not describe dispatching a microcode subroutine call operation. In fact, as described above, Tran **teaches away from** the dispatch unit dispatching a microcode subroutine call operation in response to detecting a microcoded instruction in the previous citation (instruction decode unit 36 stops dispatching instructions). Instead, this citation describes instruction decode unit 36 sending an indication of the instruction to microcode unit 45, which completes the routine. As discussed above regarding claim 1, sending an indication of an instruction is clearly not the same as dispatching a microcode subroutine call operation, as recited in Applicants' claim 29.

Finally regarding claim 29, the Examiner cites column 4, lines 42-54 as teaching that the microcode subroutine call operation pushes an address of the other instruction onto a stack, that the microcode subroutine includes a return operation, and that execution of the return operation pops the address from the stack (x86 Call instruction and x86 Return instruction). However, this citation has nothing to do with pushing or popping an instruction onto or off of a stack as part of a microcode subroutine call operation dispatched in response to detecting a microcoded instruction, as recited in claim 29. Instead it describes that subroutine call instructions (e.g., the CALL instruction of the x86 instruction set) having target addresses within a particular range of addresses are indicative of DSP functions. In this example, these DSP functions are executed by branching to a subroutine explicitly programmed using the CALL and RET instructions of the x86 instruction set. That is, the instruction detected by instruction decode unit 36 is itself a CALL instruction to a particular target address range, not a microcoded

instruction for which a microcode subroutine call operation is dispatched in response to this detection.

For at least the reasons above, the rejection of claim 29 is not supported by the cited art and removal thereof is respectfully requested.

Claim 41 includes limitations similar to claim 29, and so the arguments presented above apply with equal force to this claim, as well.

Regarding claim 40, Carbine fails to teach or suggest *dispatching one or more operations included in a first microcode subroutine and one or more operations included in a second microcode subroutine, wherein said dispatching the one or more operations in the first microcode subroutine comprises performing register name replacements using replacement register names stored in a first alias table element and wherein said dispatching the one or more operations in the second microcode subroutine comprises performing register name replacements using replacement register names stored in a second alias table element.* The Examiner cites column 12, lines 35-56, as teaching generic microcode routines, and asserts that each of these generic microcode routines "has micro-alias registers" to replace register names within the routine. The Examiner seems to be implying that these generic routines, including what he interprets as separate micro-alias registers, teach dispatching operations from both a first and second microcode subroutine, and the use of both a first and second alias table element. However, there is nothing in this citation or elsewhere in Carbine that teaches multiple alias table elements or multiple micro-alias registers. Instead, Carbine describes a single micro-alias register (having multiple fields, but not multiple entries), which is loaded with different data dependent on which of four CUOPs is selected by multiplexer 560. There is also nothing in this citation that teaches dispatching multiple microcode subroutines, as recited in claim 40. Instead, Carbine describes microcode sequencing unit 534 issuing multiple CUOPs for one microcode flow (associated with a single entry point) at a time (see, e.g., column 11, lines 11-13). Since Carbine fails to teach or suggest dispatching operations

from a first and second microcode subroutine and a first and second alias table element, Carbine cannot be said to anticipate claim 40.

For at least the reasons above, the rejection of claim 40 is not supported by the cited art and removal thereof is respectfully requested.

Applicants also assert that numerous ones of the dependent claims recite further distinctions over the cited art. However, since the rejection has been shown to be unsupported for the independent claims, a further discussion of the dependent claims is not necessary at this time.

Section 103(a) Rejection:

The Examiner rejected claims 2-6, 18-22 and 30-34 under 35 U.S.C. § 103(a) as being unpatentable over Tran in view of Carbine, claims 7, 8, 23, 24, 35 and 36 as being unpatentable over Tran and Carbine as applied to claim 2 above, and further in view of Rotenberg, et al. ("Trace Cache: a Low Latency Approach to High Bandwidth Instruction Fetching") (hereinafter "Rotenberg"), claims 9, 10, 25 and 37 as being unpatentable over Tran in view of Kling (U.S. Publication 2004/0049657), and claims 11-14, 26 and 38 as being unpatentable over Tran and Kling as applied to claim 9 above and further in view of Harris (U.S. Patent 6,260,138). Applicants respectfully traverse these rejections. However, since the rejection of the independent claims has been shown to be unsupported, as discussed above, a further discussion of the dependent claims is not necessary at this time.

CONCLUSION

Applicants submit the application is in condition for allowance, and prompt notice to that effect is respectfully requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above-referenced application from becoming abandoned, Applicants hereby petition for such an extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-81600/RCK.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Notice of Change of Address

☐ Other:

Respectfully submitted,

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